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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.      | CONFIRMATION NO. |
|---|-------------|----------------------|--------------------------|------------------|
| 10/783,314  | 02/20/2004  | Michael Warner       | TESSERA 3.0-306 II CIP I | 7827             |
| 38091   | 7590        | 09/16/2005           | EXAMINER                 |                  |
| LERNER DAVID, LITENBERG, KRUMHOLZ & MENTLIK<br>600 SOUTH AVENUE WEST<br>WESTFIELD, NJ 07090 |             |                      | SANDVIK, BENJAMIN P      |                  |
|   |             |                      | ART UNIT                 | PAPER NUMBER     |
|   |             |                      | 2826                     |                  |

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/783,314

Applicant(s)

WARNER ET AL.

Examiner

Ben P. Sandvik

Art Unit

2826

SM

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 8-12 and 14-22 is/are pending in the application.
- 4a) Of the above claim(s) 5-7, 13, 23-44 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 8-12, 14-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. ____   |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____   | 6) <input type="checkbox"/> Other: ____                                     |

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of claims 1-4, 8-12, 14-22 in the reply filed on 6/30/2005 is acknowledged.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 14-19, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Ku et al (U.S. PG Pub #20030001252).

With respect to **claim 1**, Ku teaches a first semiconductor chip (Fig. 5B, 4) having a front face, a rear face, edges bounding said faces and contacts exposed at said front face (Fig. 5B, 13); a second chip (Fig. 5B, 2), said second chip having front and rear surfaces and contacts on said front surface (Fig. 5B, 13), at least some of the contacts on said second chip being electrically connected to at least some of said contacts on said first chip (Fig. 5B, 13), said front surface of said second chip facing upwardly and confronting a face of said first chip (Fig. 5B, 2a); a chip carrier disposed below said rear surface of said

second chip (Fig. 5B, 12), said chip carrier having a bottom surface facing downwardly away from said second chip and having a plurality of terminals exposed at said bottom surface for connection to a circuit panel (Fig. 5B, 20), at least some of said terminals being electrically connected to at least one of said chips (Paragraph 40), said chip carrier further having an opening coinciding with at least a portion of said rear surface of said second chip (Fig. 5B, 12b), said opening being sized and disposed to coincide with a thermally conductive element of the circuit panel when said packaged semiconductor chip is mounted to the circuit panel (Fig. 5B, 10).

With respect to **claim 14**, Ku teaches a configuration wherein a rear face of a first chip (Fig. 1, 17) faces downwardly towards said front surface of said second chip (Fig. 1, 15).

With respect to **claim 15**, Ku teaches leads connecting at least some of the contacts of said first chip and at least some of said contacts of said second chip (Fig. 5B, 6).

With respect to **claim 16**, Ku teaches a thermally conductive layer between said rear face of said first chip and said front face of said second chip (Fig. 1, 16).

With respect to **claim 17**, Ku teaches that said front face of said first chip faces (Fig. 5B, 4) downwardly towards said front surface of said second chip (Fig. 5B, 2).

With respect to **claim 18**, Ku teaches that said contacts of said first chip are bonded to said contacts of said second chip, said first chip being in thermal communication with said second chip through said bonded contacts (Fig. 5B, 6).

With respect to **claim 19**, Ku teaches a thermally conductive underfill between said first and second chips, said first chip being in thermal communication with said second chip through said underfill (Fig. 5B, 18).

With respect to **claim 21**, Ku teaches that said thermal conductor and said terminals are adapted for surface mounting to a circuit board (Paragraph 53, "thermally and/or connected to a motherboard").

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ku, in view of Ho et al (U.S. Patent #6657296).

With respect to **claim 2**, Ku teaches all of the limitations of claim 1, but does not teach a circuit panel including the thermally conductive element, and thermally conductive material connecting said rear surface of said second chip to said thermally conductive element of said circuit panel such that said rear surface of said second chip thermally communicates with said circuit panel through said

thermally conductive material. Ho teaches a circuit panel mounted to a bottom surface of a chip carrier (Fig. 5, 59), a thermally conductive element (Fig. 5, 581), and a thermally conductive material connecting the chip carrier to the thermally conductive element (Fig. 5, 580). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the thermally conductive element of Ku on a circuit panel and to use a thermally conductive material to connect the rear surface of the second chip to the thermally conductive element as taught by Ho in order to enhance the thermal performance of the package.

With respect to **claim 3**, Ku and Ho teach all of the limitations of claim 2, but Ku does not teach a thermally conductive material including solder. Ho teaches a thermally conductive material that includes solder (Col 4 Ln 46-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a material that includes solder as taught by Ho in order to enhance the thermal performance of the package.

With respect to **claim 4**, Ku and Ho teach all of the limitations of claim 2, but Ku does not teach a thermally conductive material including thermally conductive paste. Ho teaches a thermally conductive material that includes thermally conductive paste (Col 4 Ln 46-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a material that includes thermally conductive paste as taught by Ho in order to enhance the thermal performance of the package.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ku, in view of Bonis (U.S. Patent #5187122).

With respect to **claim 8**, Ku teaches all of the limitations of claim 1, but does not teach that said second chip includes a plurality of passive electrical components. Bonis teaches an integrated circuit with a plurality of passive electrical components (Col 1 Ln 9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the second chip of Ku with a plurality of passive electrical components as taught by Bonis in order to use the package to process logic and analog signals.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ku and Bonis, in view of Hofstee (U.S. PG Pub #20020074668).

With respect to **claim 9**, Ku and Bonis teach all of the limitations of claim 8, but do not teach a plurality of second chips. Hofstee teaches a configuration wherein a plurality of bottom chips (Fig. 2, 206) are provided under a top chip (Fig. 2, 204). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the package of Ku and Bonis with a plurality of second chips in order to increase the number of function that can be performed by the package.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ku, in view of Li (U.S. PG Pub #20020195700).

With respect to **claim 10**, Ku teaches all of the limitations of claim 1, but does not teach one or more discrete passive electrical components electrically connected to the terminals of said chip carrier. Li teaches a package with discrete passive electrical components connected to a chip carrier (Fig. 5, 506). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect passive components to the terminals of Ku as taught by Li in order to suppress unwanted radiation.

With respect to **claim 11**, Ku teaches all of the limitations of claim 1, but does not teach one or more discrete passive electrical components electrically connected to at least one of said chips. Li teaches a package with discrete passive electrical components electrically connected to a chip (Fig. 5, 504). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect passive components at least one of the chips of Ku as taught by Li in order to suppress unwanted radiation.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ku, in view of Tsai et al (U.S. PG Pub #20040041249).

With respect to **claim 12**, Ku teaches all of the limitations of claim 1, but does not teach that each of the faces of said first chip has a first area, and said opening of said chip carrier coincides with said rear surface of said second chip



over a second area larger than said first area. Tsai teaches a configuration where an opening of a chip carrier coincides with a rear surface of a bottom chip (Fig. 2, 20) over a greater area than a width of a top chip (Fig. 2, 34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the package of Ku with the configuration taught by Tsai in order to decrease the size of the package.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ku, in view of Dotta et al (U.S. Patent #6353263).

With respect to **claim 20**, Ku teaches all of the limitations of claim 1, but does not teach that the chip carrier is a sheet-like element having thickness less than about 150 microns. Dotta teaches a chip carrier that sheet-like element having thickness less than about 150 microns (Fig. 1, 20 and Col 8 Ln 30-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the chip carrier of Ku to be about 150 microns as taught by Dotta in order to make a package with a slim profile.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ku, in view of Kuan et al (U.S. PG Pub #20030047797).

With respect to **claim 22**, Ku teaches all of the limitations of claim 1, but does not teach that said first chip is a radio frequency amplifier chip. Kuan teaches a chip that is used as radio frequency amplifier chip (Paragraph 24). It

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would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first chip of Ku a radio frequency amplifier chip as taught by Kuan in order to use the package to process a signal.

  
NATHAN J. FLYNN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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